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In re the Application of: **Masaro IIDA**

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For: **DATA SEQUENCE CONVERSION CIRCUIT AND PRINTER USING THE SAME**

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Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Date: June 3, 2005

Sir:

Submitted herewith is a verified translation of the certified copy of the foreign priority document for the above-identified application. This translation is being submitted to overcome the 35 U.S.C. §102 rejection and one of the 35 U.S.C. §103 rejections in the Office Action of February 24, 2005.

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Respectfully submitted,

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In re Patent Application of: Masaru Iida

Serial No. 09/839,370 Examiner: PAHM, HAI CHI
Filed: April 23, 2001 Group Art Unit: 2861
For: DATA SEQUENCE CONVERSION CIRCUIT AND PRINTER USING THE SAME

TRANSLATOR'S DECLARATION

Honorable Commissioner of Patents & Trademarks
Washington, D.C. 20231

Sir:

I, Masami Enohara , residing at c/o A. AOKI, ISHIDA & ASSOCIATES, Toranomon 37 Mori Bldg., 3-5-1, Toranomon Minato-ku, Tokyo 105-8423, Japan declare the following:

(1) That I know well both the Japanese and English languages;

(2) That I translated Japanese Patent Application No. 2000-402150, filed December 28, 2000 , from the Japanese language to the English language;

(3) That the attached English translation is a true and correct translation of the aforesaid Japanese Patent Application No. 2000-402150 to the best of my knowledge and belief; and

(4) That all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereon.

May 27, 2005
Date

Masami Enohara
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[TITLE OF THE INVENTION] DATA SEQUENCE CONVERSION CIRCUIT AND PRINTER USING THE SAME

[NUMBER OF CLAIMS] 5

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[Name of Article]	Drawing	1
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[NAME OF DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] DATA SEQUENCE CONVERSION CIRCUIT AND PRINTER USING THE SAME

[SCOPE OF CLAIM FOR PATENT]

[Claim 1] A data sequence conversion circuit which takes as an input any one of a plurality of input data sequences having different data widths, and which converts said input data sequence into an output data sequence having a prescribed data width for output, said circuit comprising:

a first parallel shift register for holding said input data sequence;

a switch matrix for taking the data held in said first parallel shift register as input data, and for outputting said input data in a distributed fashion in accordance with a rule selected by a control signal from a plurality of predetermined rules; and

a second parallel shift register for taking the data output from said switch matrix as input data, and for outputting said input data as a data sequence having said prescribed data width.

[Claim 2] A data sequence conversion circuit as claimed in claim 1, wherein when the data widths of said plurality of input data sequences are denoted by Wn (n = 1, 2, 3, ...), respectively, and the data width of said output data sequence by Wo, said first parallel shift register has a data width at least equal to the largest value of Wn (n = 1, 2, 3, ...), and has the number of stages at least equal to the largest value of the quotients QIn (n = 1, 2, 3, ...) each obtained by dividing the least common multiple of Wn (n = 1, 2, 3, ...) and Wo by Wn.

[Claim 3] A data sequence conversion circuit as claimed in claim 1, wherein when the data widths of said plurality of input data sequences are denoted by Wn (n = 1, 2, 3, ...), respectively, and the data width of said output data sequence by Wo, said second parallel shift register has the

number of stages at least equal to the largest value of the quotients QOn (n = 1, 2, 3, ...) each obtained by dividing the least common multiple of Wn (n = 1, 2, 3, ...) and Wo by Wo.

[Claim 4] A data sequence conversion circuit as claimed in claim 1, wherein when the data width of said input data sequence is denoted by Wn, and the data width of said output data sequence by Wo, said switch matrix outputs said input data so that Wn×QIn units of data input and held in the first stage to the (QIn)th stage in said first parallel shift register as counted from the input side thereof are input to the first stage to the (QOn)th stage in said second parallel shift register as counted from the output side thereof, where QIn is the quotient of the least common multiple of Wn and Wo divided by Wn, and QOn is the quotient of the least common multiple of Wn and Wo divided by Wo.

[Claim 5] A printer comprising a data sequence conversion circuit as claimed in any one of claims 1-5, said data sequence circuit being located between a jaggy correction circuit and a line-like printhead.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a data sequence conversion circuit for converting a plurality of input data sequences having different data widths into output data sequences having a prescribed data width, and also relates to a printer using the same.

[0002]

[Prior Art]

An LED printer is a form of electrophotographic image forming apparatus, and uses an LED array head as a means for exposing optical image information onto a photosensitive drum. Such an LED array head comprises: an LED array consisting of a row of LEDs arranged at prescribed pitch; a shift register consisting of storage elements each for storing one image data

unit corresponding to one LED, the number of storage elements being the same as the number of LEDs; and an LED driving circuit for driving the LEDs to emit light in accordance with the image data stored in the shift register.

[0003]

With increasing LED printer speed, and with increasing resolution and printing width, the amount of image data, that is transferred into the register section of the LED array head within a unit time, has increased. To increase the speed of image data transfer to the register section without increasing the transfer clock frequency of the shift register, the LED array head employs a parallel shift register configuration in which a sequence of image data corresponding to the plurality of LEDs is input simultaneously in parallel form.

[0004]

The printing resolution of an LED printer is determined by the pitch of the LED arrangement. Japanese Unexamined Patent Publication No. 7-156442 discloses an LED printer that uses an LED array consisting of LEDs arranged at a pitch corresponding to the pixel pitch of resolution equal to the least common multiple of a plurality of different resolutions. For example, image data of resolutions 240 dpi, 300 dpi, and 400 dpi are printed using an LED array head having a resolution of 1200 dpi which is the least common multiple of the image data resolutions.

[0005]

The above Unexamined Patent Publication number also discloses an LED printer in which, using the fact that one pixel unit of low resolution print data is formed by a plurality of LEDs, control is performed to add smaller print dots around an attention pixel or erase smaller print dots from an attention pixel by individually and selectively lighting or extinguishing the LEDs forming the pixel unit. That is, the LED printer disclosed therein has the function of correcting for jagged edges (jaggies) that appear when printing a low

resolution image.

[0006]

[Problems to be Solved by the Invention]

In an LED printer that prints low resolution print data of 240 dpi, 300 dpi, and 400 dpi using an LED array head having a resolution of 1200 dpi which is the least common multiple of the print data resolutions, one dot of print image data of 240 dpi is formed from five print dots of 1200 dpi, one dot of print image data of 300 dpi is formed from four print dots of 1200 dpi, and one dot of print image data of 400 dpi is formed from three print dots of 1200 dpi. When the jaggy correction method described above is applied to this LED printer, a jaggy correction circuit determines a pattern of five, four, or three high resolution print dots, respectively, and outputs the pattern at the attention dot position of the low resolution print data of 240 dpi, 300 dpi, or 400 dpi, respectively. That is, one unit of data output from the jaggy correction circuit varies depending on the resolution of the input low resolution print image data.

[0007]

If an LED array head employing a parallel shift register configuration is used as the LED array head of 1200 dpi, the data width of the parallel input to the LED array head does not necessarily coincide with the width of the print dot pattern that the jaggy correction circuit outputs. Data sequence conversion is therefore needed for converting the output data sequence of the jaggy correction circuit, which varies depending on the input image data resolution, into a data sequence that matches the data width of the parallel input to the LED array head.

[0008]

A data sequence conversion circuit may be constructed using a PS conversion circuit, which applies a parallel-to-serial conversion to the output data of the jaggy correction circuit, and an SP conversion circuit, which applies a serial-

to-parallel conversion to the PS converted output so as to match the parallel input data width of the LED array head, and the data sequence conversion may be accomplished by applying a suitable control signal (clock signal).

[0009]

However, in the data sequence conversion circuit of the above configuration, since the print dot data is first converted into serial data, this is equivalent to serially transferring the high resolution print dot data. Accordingly, the data conversion circuit must be constructed using high speed operating shift registers, defeating the purpose of the LED array head of the parallel shift register configuration in which the print dot data are input in parallel in order to increase the print speed without increasing the frequency of the shift register transfer clock.

[0010]

The present invention has been devised in view of the above problem, and an object of the invention is to provide a data sequence conversion circuit for converting a plurality of input data sequences having different data widths into output data sequences having a prescribed data width without converting them into serial data. It is another object of the present invention to provide an LED printer that uses such a data sequence conversion circuit.

[0011]

[Means for Solving the Problem]

To achieve the above objects, according to the present invention, there is provided a data sequence conversion circuit which takes as an input any one of a plurality of input data sequences having different data widths, and which converts the input data sequence into an output data sequence having a prescribed data width for output, the circuit comprising: a first parallel shift register for holding the input data sequence; a switch matrix for taking the data held in the first parallel shift register as input data, and for outputting the

input data in distributing fashion in accordance with a rule selected by a control signal from a plurality of predetermined rules; and a second parallel shift register for taking the data output from the switch matrix as input data, and for outputting the input data as a data sequence having the prescribed data width.

[0012]

In the above configured data sequence conversion circuit, any one of the plurality of input data sequences having different data widths is held in the first parallel shift register. Then, the data held in the first parallel shift register is read as input data into the switch matrix, and is output from the switch matrix in distributing fashion in accordance with a rule selected by a control signal from a plurality of predetermined rules. The thus output data is input into the second parallel shift register which outputs a data sequence having the prescribed data width. In this way, the desired data sequence conversion can be accomplished without converting the input data sequence into serial data.

[0013]

Preferably, according to the present invention, when the data widths of the plurality of input data sequences are denoted by Wn (n = 1, 2, 3, ...), respectively, and the data width of the output data sequence by Wo, the first parallel shift register has a data width at least equal to the largest value of Wn (n = 1, 2, 3, ...), and has the number of stages at least equal to the largest value of the quotients QIn (n = 1, 2, 3, ...) each obtained by dividing the least common multiple of Wn (n = 1, 2, 3, ...) and Wo by Wn.

[0014]

Preferably, according to the present invention, when the data widths of the plurality of input data sequences are denoted by Wn (n = 1, 2, 3, ...), respectively, and the data width of the output data sequence by Wo, the second parallel shift register has the number of stages at least equal to the

largest value of the quotients QOn (n = 1, 2, 3, ...) each obtained by dividing the least common multiple of Wn (n = 1, 2, 3, ...) and Wo by Wo.

[0015]

Preferably, according to the present invention, when the data width of the input data sequence is denoted by Wn, and the data width of the output data sequence by Wo, the switch matrix outputs the input data so that Wn×QIn units of data input and held in the first stage to the (QIn)th stage in the first parallel shift register as counted from the input side thereof are input to the first stage to the (QOn)th stage in the second parallel shift register as counted from the output side thereof, where QIn is the quotient of the least common multiple of Wn and Wo divided by Wn, and QOn is the quotient of the least common multiple of Wn and Wo divided by Wo.

[0016]

Furthermore, according to the present invention, there is provided a printer having the above-described data sequence conversion circuit which is located between a jaggy correction circuit and a line-like printhead. In this printer, high resolution image data can be transferred into the shift register section of the line-like printhead without increasing the frequency of the shift register transfer clock.

[0017]

[Best Mode for Carrying Out the Invention]

An embodiment of the present invention will be described below with reference to the accompanying drawings.

[0018]

Figure 1 is a diagram schematically showing the construction of a printing section in an LED printer to which the data sequence conversion circuit of the present invention can be applied. The printing section 20 comprises: a photosensitive drum 22 as an image carrier located at the center; a charging unit 24 for applying electrical charges to the surface of the photosensitive drum; an LED array head 26 as

an exposure unit for forming a latent image; a developing unit 28 for forming a toner image by making the latent image visible using a developer; a transfer unit 30 for transferring the developed toner image onto an image recording medium; a charge erasing unit 32 for erasing charges remaining on the surface of the photosensitive drum; and a cleaner 34 for removing toner remaining on the photosensitive drum after the transfer of the toner image.

[0019]

Figure 2 is a diagram of an LED array as viewed from the photosensitive drum 22 side, and Figure 3 is a diagram showing the configuration of a serial data input type LED array head. As shown in these figures, the LED array head 26 in Figure 1 comprises: an LED array 40 consisting of a row of LEDs arranged at a prescribed pitch; a shift register 44 consisting of storage elements (flip-flops) each for storing one image data unit corresponding to one LED, the number of storage elements being the same as the number of LEDs; and an LED driving circuit 42 for driving the LEDs to emit light in accordance with the image data stored in the shift register. The flip-flop located at the innermost end of the shift register 44 corresponds to the leftmost LED in Figure 2. That is, the positional relationship of the LEDs is reversed left and right between Figure 2 and Figure 3.

[0020]

Figure 4 is a diagram showing the configuration of a parallel data input type LED array head. As previously noted, with increasing LED printer speed, and with increasing resolution and printing width, the amount of image data that is transferred into the shift register of the LED array head within a unit time increases. To increase the speed of image data transfer to the shift register without increasing the transfer clock frequency of the shift register, the LED array head employs a parallel shift register configuration in which a sequence of image data corresponding to the plurality of LEDs

is input simultaneously in parallel form. In the example of Figure 4, an 8-bit parallel shift register 46 is used. The high-order bit of the 8-bit parallel data corresponds to the leading bit of serial data (the innermost bit in the case of a serial shift register, or the leftmost LED in the LED array of Figure 2).

[0021]

Figure 5 is a diagram showing the configuration of a jaggy correction circuit. As previously stated, the printing resolution of an LED printer is determined by the pitch of the LED arrangement. However, in the case of an LED printer that uses an LED array consisting of LEDs arranged at a pitch corresponding to the pixel pitch of resolution equal to the least common multiple of a plurality of different resolutions (for example, a printer that prints image data of 240 dpi, 300 dpi, and 400 dpi by using an LED array head of 1200 dpi which is the least common multiple of the image data resolutions), use is made of the fact that one pixel unit of low resolution print data is formed by a plurality of LEDs, and control is performed to add smaller print dots around an attention pixel or erase smaller print dots from the attention pixel by individually and selectively lighting or extinguishing the LEDs forming the pixel unit, thereby eliminating jagged edges or jaggies that appear when printing a low resolution image.

[0022]

In the jaggy correction circuit 50 illustrated in Figure 5, low resolution print data expanded in an image memory 48 is read into a line buffer 54 by an image memory reading unit 52. An evaluation window extracting unit 56 extracts an attention dot and its neighboring rectangular regions as an evaluation window from the line buffer 54. A corrected image data generating unit 58 determines, from the pattern extracted as the evaluation window, a high resolution print dot pattern with smaller print dots added or erased at the attention dot position, and outputs the thus determined pattern as corrected

image data.

[0023]

Figure 6 is diagrams for explaining the operation of the jaggy correction circuit, illustrating an example of how the print dot pattern is determined in the jaggy correction circuit 50 of Figure 5. From the pattern of Figure 6(A) which is a portion extracted from the low resolution print data, the corrected high resolution print dot pattern at the attention dot position in the center of the extracted region is determined as shown in Figure 6(B). By repeating a similar correction process, the low resolution print pattern of the shape shown in Figure 6(A) is corrected to the high resolution print dot pattern shown in Figure 6(C).

[0024]

Figure 7 is a block diagram for explaining the data sequence conversion circuit of the present invention in relation to other circuits. As previously described, in an LED printer that prints low resolution print data of 240 dpi, 300 dpi, and 400 dpi using an LED array head having a resolution of 1200 dpi which is the least common multiple of the print data resolutions, one dot of print image data of 240 dpi is formed from five print dots of 1200 dpi, one dot of print image data of 300 dpi is formed from four print dots of 1200 dpi, and one dot of print image data of 400 dpi is formed from three print dots of 1200 dpi.

[0025]

The jaggy correction circuit 50 (Figure 5), which is provided in such an LED printer, determines a pattern of five, four, or three high resolution print dots, respectively, and outputs the pattern at the attention dot position of the low resolution print data of 240 dpi, 300 dpi, or 400 dpi, respectively. That is, the output unit of the jaggy correction circuit 50 varies depending on the resolution of the input low resolution print image data.

[0026]

If an LED array head employing a parallel shift register configuration is used as the LED array head of 1200 dpi, the data width (8 bits in the example of Figure 4) of the parallel input to the LED array head 26 does not necessarily coincide with the width of the print dot pattern that the jaggy correction circuit 50 outputs. Therefore, the data sequence conversion circuit 60 for converting the output data sequence of the jaggy correction circuit 50, which varies depending on the input image data resolution, into a data sequence having a data width that matches the parallel input to the LED array head 26, must be provided between the jaggy correction circuit 50 and the LED array head 26, as shown in Figure 7.

[0027]

Figure 8 is a diagram showing the configuration of a prior art data sequence conversion circuit. This prior art circuit comprises a PS conversion circuit 62, which applies a parallel-to-serial conversion to the output data of the jaggy correction circuit 50, and an SP conversion circuit 64, which applies a serial-to-parallel conversion to the PS converted output so as to match the parallel input data width of the LED array head, and a suitable control signal (clock signal) is applied for the operation of the circuit. In the example of Figure 8, a data sequence of 5-bit width is converted into a data sequence of 8-bit width.

[0028]

However, in the data sequence conversion circuit of Figure 8, since the print dot data is first converted into serial data, this is equivalent to serially transferring the high resolution print dot data. Accordingly, the data conversion circuit must be constructed using high speed operating shift registers, defeating the purpose of the LED array head of the parallel shift register configuration in which the print dot data are input in parallel in order to increase the print speed without increasing the frequency of the shift register transfer clock.

[0029]

Consider, for example, the case where a continuous sheet printer of 10,000 lines (line height of about 0.42 cm or 1/6 inch) and print width of 43.18 cm (17 inches), equipped with an LED array head of 1200 dpi, prints low resolution print data of 240 dpi, 300 dpi, and 400 dpi by converting them to 1200 dpi. In the case of an LED array head that does not employ a parallel data input configuration, the data transfer frequency F of the LED array head is given as follows.

240 dpi: F > 136.0 MHz

300 dpi: F > 170.0 MHz

400 dpi: F > 226.6 MHz

On the other hand, in the case of an LED array head of 8-bit parallel data input type, the data transfer frequency F can be reduced by a factor of 8, compared with the above frequency. However, in the case of the data sequence conversion circuit of Figure 8, the same frequency as given above is required to operate the shift registers of the PS conversion circuit and SP conversion circuit.

[0030]

Figure 9 is a diagram showing one embodiment of the data sequence conversion circuit of the present invention, which is devised to overcome the above problem. The data sequence conversion circuit 60 is applicable for use in an LED printer in which low resolution print data of 240 dpi, 300 dpi, and 400 dpi are corrected for jaggies and are printed using a 1200 dpi LED array head of 8-bit parallel input type.

[0031]

The jaggy correction circuit for correcting jaggies in the low resolution print data of 240 dpi, 300 dpi, or 400 dpi determines and outputs a pattern of five, four, or three high resolution print dots, respectively, by correcting print dots at the attention dot position of the low resolution print data. At this time, the jaggy correction circuit shown in Figure 5 outputs a 5-bit, 4-bit, or 3-bit data sequence as the print dot

correction at the attention dot position of the low resolution print data progresses.

[0032]

The jaggy correction circuit 50 is constructed as a circuit capable of outputting five bits, the largest bit count of the high resolution output dot patterns, and the corrected image data generating unit is configured to generate a pattern appropriate to the input resolution; in this way, the same jaggy correction circuit can be used for the various resolutions.

[0033]

To convert input data sequences of 5-bit width into output data sequences of 8-bit width, the input data as parallel data should be converted in blocks of 40 bits which is the least common multiple of the input and output data widths, that is, input 5 bits × 8 are together converted into 8 bits × 5. Likewise, to convert input data sequences of 4-bit width into output data sequences of 8-bit width, 8 bits are treated as one unit, and input 4 bits × 2 are together converted into 8 bits × 1; similarly, to convert input data sequences of 3-bit width into output data sequences of 8-bit width, 24 bits are treated as one unit, and the input 3 bits × 8 are together converted into 8 bits × 3.

[0034]

Accordingly, in the circuit shown in Figure 9, an input shift register 72 needs to have a data width of 5 bits which is equal to the largest bit width of the input data sequence. Further, the input shift register 72 needs to have eight stages, the largest number of stages necessary for input. On the other hand, an output shift register 76 needs to have five stages, the largest number of stages necessary for output.

[0035]

In Figure 9, the input shift register 72 is constructed from eight stages of register FFs i1 to i8 each having a 5-bit width. The 40 bits of data held in the input shift register 72

are read into a switch matrix 74. The data read into the switch matrix 74 are output to the output shift register 76 in accordance with a rule described later. The output shift register 76 is constructed from five stages of register FFs o1 to o5 each having an 8-bit width which is equal to the parallel input data width of the LED array head 26.

[0036]

Each of the register FFs o1 to o5 forming the output shift register 76 selects, based on a LOADa signal, whether to take and hold data input to its Da terminal from an output of the switch matrix 74 or data input to its Db terminal from a Q output at the preceding stage. In the present embodiment, when the LOADa signal is high, the data applied at the Da terminal is latched into the register FF by the input clock while, when the LOADa signal is low, the data applied at the Db terminal is latched into the register FF by the input clock.

[0037]

When correcting the low resolution print data of 240 dpi for jaggies and printing the data with the LED array head of 1200 dpi, the jaggy correction circuit outputs a high resolution print dot pattern data sequence of 5-bit width. In the data sequence conversion circuit 60 shown in Figure 9, when 5 bits × 8 stages = 40 bits of data are input and held in the input shift register 72, the input data, output from the switch matrix 74 for distribution in accordance with a suitable rule, are latched into the output shift register 76, and the data latched into the output shift register 76 are output in sequence for transfer to the LED array head 26. By repeating this process, input data sequences of 5-bit width can be converted into output data sequences of 8-bit width.

[0038]

This series of conversion operations is illustrated in timing chart form in Figure 10. As can be seen from the figure, the data sequence conversion process can be performed in sequence by repeating shift operations using clocks such

that data of five stages are output from the output shift register while data are being input into the eight stages of the input shift register. Accordingly, the ratio of the frequency of shift clock φ1 applied to the input shift register 72 to the frequency of shift clock φ2 applied to the output shift register 76 is 8:5.

[0039]

On the other hand, when correcting the low resolution print data of 300 dpi for jaggies and printing the data with the LED array head of 1200 dpi, the jaggy correction circuit outputs a high resolution print dot pattern data sequence of 4-bit width. In the data sequence conversion circuit 60 shown in Figure 9, when 4 bits × 2 stages = 8 bits of data are input and held in the input shift register 72, the input data, output from the switch matrix 74 for distribution in accordance with a suitable rule, are latched into the output shift register 76, and the data latched into the output shift register 76 are output in sequence for transfer to the LED array head 26. By repeating this process, input data sequences of 4-bit width can be converted into output data sequences of 8-bit width.

[0040]

This series of conversion operations is illustrated in timing chart form in Figure 11. As can be seen from the figure, the data sequence conversion process can be performed in sequence by repeating shift operations using clocks such that data is output from one stage of the output shift register while data are being input into the two stages of the input shift register. Accordingly, the ratio of the frequency of shift clock φ1 applied to the input shift register to the frequency of shift clock φ2 applied to the output shift register is 2:1.

[0041]

Further, when correcting the low resolution print data of 400 dpi for jaggies and printing the data with the LED array

head of 1200 dpi, the jaggy correction circuit outputs a high resolution print dot pattern data sequence of 3-bit width. In the data sequence conversion circuit 60 shown in Figure 9, when 3 bits × 8 stages = 24 bits of data are input and held in the input shift register 72, the input data, output from the switch matrix 74 for distribution in accordance with a suitable rule, are latched into the output shift register 76, and the data latched into the output shift register 76 are output in sequence for transfer to the LED array head 26. By repeating this process, input data sequences of 3-bit width can be converted into output data sequences of 8-bit width.

[0042]

This series of conversion operations is illustrated in timing chart form in Figure 12. As can be seen from the figure, the data sequence conversion process can be performed in sequence by repeating shift operations using clocks such that data of three stages are output from the output shift register while data are being input into the eight stages of the input shift register. Accordingly, the ratio of the frequency of shift clock φ1 applied to the input shift register to the frequency of shift clock φ2 applied to the output shift register is 8:3.

[0043]

The data distribution rule employed in the switch matrix 74 will be explained with reference to the example of Figure 9. In the following description, the bits of the 5-bit print dot data loaded into the input shift register 72 are designated by D4 to D0, where D0 is the dot printed at the right-hand side (which, in Figure 2, corresponds to the LED at the right-hand side and, in Figure 3 or 4, corresponds to the LED at the left-hand side). It is also assumed that D4 to D0, D3 to D0, and D2 to D0 are input as effective print dot data for jaggy correction at 240 dpi, 300 dpi, and 400 dpi, respectively. The bits of the data (Q outputs) held in the respective FFs iN (N = 1, 2, ..., 8) are designated by FF iN-Q4 to FF iN-Q0,

respectively. Further, the bits at the switch matrix output terminals connected to the Da input terminals of the respective FFs oN (N = 1, 2, ..., 5) are designated by FF oN-Da7 to FF oN-Da0 in a relationship corresponding to the respective bits of the output shift register, where Da0 represents the dot printed at the right-hand side.

[0044]

Figure 13 shows the distributing output rule used in the switch matrix 74 when correcting the low resolution print data of 240 dpi for jaggies and printing the data with the LED array head of 1200 dpi. The figure shows the relationship between the switch matrix output data coupled to the respective Da input terminals of the output shift register and the Q outputs of the input shift register coupled into the switch matrix. For example, FF i8-Q4 (the leading bit of the input 40 bits) output from the input shift register 72 is applied at FF o5-Da7 of the output shift register 76 via the switch matrix 74.

[0045]

Likewise, Figures 14 and 15 show the distributing output rules used in the switch matrix when correcting the low resolution print data of 300 dpi and 400 dpi for jaggies and printing the respective data with the LED array head of 1200 dpi. In each figure, the mark "x" means that the output data is not specifically specified (that is, not needed in the data sequence conversion of the present embodiment). As can be seen from these figures, the necessary number of stages, counting from the input side, are used in the input shift register, while in the output shift register, the necessary number of stages, counting from the output side, are used.

[0046]

Figures 16, 17, 18, 19, and 20 are diagrams showing an example of the circuit configuration of the switch matrix 74. The circuits shown in these figures are combined to form a single switch matrix circuit. The circuits in these figures are shown using simplified designations, and Figure 21 are

diagrams for explaining the designations. That is, the circuit shown in Figure 21(A) in simplified form actually represents the circuit shown in Figure 21(B).

[0047]

In these figures, SL-240, SL-300, SL-400, and FF iN-QX (N = 1, 2, ..., 8; Q = 0, 1, ..., 4) are input signals to the switch matrix 74, and FF oM-DaY (M = 1, 2, ..., 5; Y = 0, 1, ..., 7) are output signals from the switch matrix 74.

[0048]

More specifically, SL-240, SL-300, and SL-400 are resolution selection signals, an appropriate one of which goes high depending on the low resolution print data to be corrected for jaggies; that is, SL-240 goes high when data of 240 dpi is input, SL-300 goes high when data of 300 dpi is input, and SL-400 goes high when data of 400 dpi is input.

[0049]

The input signals FF iN-QX (N = 1, 2, ..., 8; Q = 0, 1, ..., 4) to the switch matrix 74 are the signals supplied from the corresponding Q outputs of the FF i1 to FF i8 in the input shift register 72 shown in Figure 9. The output signals FF oM-DaY (M = 1, 2, ..., 5; Y = 0, 1, ..., 7) from the switch matrix 74 are the signals applied to the corresponding Da inputs of the FF o1 to FF o5 in the output shift register 76 shown in Figure 9.

[0050]

The operation of the switch matrix circuit 74 shown in Figures 16, 17, 18, 19, and 20 will be described by reference to the portion thereof shown in Figure 21. When the resolution of the low resolution print data input to the jaggy correction circuit is 240 dpi, the resolution selection signal SL-240 goes high, and an output signal from Q1 of FF i8 in the input shift register 72 is applied to Da4 of FF o5 in the output shift register 76.

[0051]

Likewise, when the resolution of the low resolution print

data input to the jaggy correction circuit is 300 dpi, the resolution selection signal SL-300 goes high, and an output signal from Q0 of FF i2 in the input shift register 72 is applied to Da4 of FF o5 in the output shift register 76. Further, when the resolution of the low resolution print data input to the jaggy correction circuit is 400 dpi, the resolution selection signal SL-400 goes high, and an output signal from Q2 of FF i7 in the input shift register 72 is applied to Da4 of FF o5 in the output shift register 76.

[0052]

As described above, according to the present embodiment, since, in the input and output shift registers, data are shifted by at least 3-bit width, input data sequences of different data width can be converted into output sequences of prescribed data length while holding the operating frequency low for the shift registers that perform the data sequence conversion. At this time, by varying the distributing output rule in the switch matrix and the ratio of the shift clock frequencies for the input and output shift registers, input data sequences of different data widths can be handled. In the present embodiment, the output data of the data sequence conversion circuit has been described as being transferred directly to the LED array head; alternatively, the output data may be stored temporarily in a memory having a prescribed bit width.

[0053]

The present embodiment has been described dealing with a printer having an LED array head, but the invention is applicable to any type of printer that has a line-like printhead and drives memory devices based on data loaded into a shift register.

[0054]

The present invention has been described with reference to the preferred embodiments. Concrete preferred modes of the present invention will be added below.

[0055]

(Addition 1) A data sequence conversion circuit which takes as an input any one of a plurality of input data sequences having different data widths, and which converts said input data sequence into an output data sequence having a prescribed data width for output, said circuit comprising:

a first parallel shift register for holding said input data sequence;

a switch matrix for taking the data held in said first parallel shift register as input data, and for outputting said input data in a distributed fashion in accordance with a rule selected by a control signal from a plurality of predetermined rules; and

a second parallel shift register for taking the data output from said switch matrix as input data, and for outputting said input data as a data sequence having said prescribed data width. (1)

[0056]

(Addition 2) A data sequence conversion circuit according to addition 1, wherein when the data widths of said plurality of input data sequences are denoted by Wn (n = 1, 2, 3, ...), respectively, and the data width of said output data sequence by Wo, said first parallel shift register has a data width at least equal to the largest value of Wn (n = 1, 2, 3, ...), and has the number of stages at least equal to the largest value of the quotients QIn (n = 1, 2, 3, ...) each obtained by dividing the least common multiple of Wn (n = 1, 2, 3, ...) and Wo by Wn. (2)

[0057]

(Addition 3) A data sequence conversion circuit according to addition 1, wherein when the data widths of said plurality of input data sequences are denoted by Wn (n = 1, 2, 3, ...), respectively, and the data width of said output data sequence by Wo, said second parallel shift register has the number of stages at least equal to the largest value of the

quotients QOn (n = 1, 2, 3, ...) each obtained by dividing the least common multiple of Wn (n = 1, 2, 3, ...) and Wo by Wo. (3)

[0058]

(Addition 4) A data sequence conversion circuit according to addition 1, wherein the data widths of said plurality of input data sequences are 5 bits, 4 bits, and 3 bits, respectively, the data width of said output data sequence is 8 bits, said first parallel shift register has a 5-bit data width and eight stages, and said second parallel shift register has five stages.

[0059]

(Addition 5) A data sequence conversion circuit according to addition 1, wherein when the data width of said input data sequence is denoted by Wn, and the data width of said output data sequence by Wo, said switch matrix outputs said input data so that Wn×QIn units of data input and held in the first stage to the (QIn)th stage in said first parallel shift register as counted from the input side thereof are input to the first stage to the (QOn)th stage in said second parallel shift register as counted from the output side thereof, where QIn is the quotient of the least common multiple of Wn and Wo divided by Wn, and QOn is the quotient of the least common multiple of Wn and Wo divided by Wo. (4)

[0060]

(Addition 6) A data sequence conversion circuit according to addition 1, wherein when the data width of said input data sequence is denoted by Wn, and the data width of said output data sequence by Wo, the shift clock frequency Fi of said first parallel shift register and the shift clock frequency Fo of said second parallel shift register have a relation defined by Fi/Fo = Wo/Wn.

[0061]

(Addition 7) A data sequence conversion circuit according to addition 1, wherein when the data width of said

input data sequence is denoted by Wn, and the data width of said output data sequence by Wo, each time QIn data sequences are input into said first parallel shift register, Wn×QIn units of data are input into said second parallel shift register via said switch matrix, following which QOn data sequences are output from said second parallel shift register.

[0062]

(Addition 8) A printer comprising a data sequence conversion circuit according to any one of additions 1-7, said data sequence circuit being located between a jaggy correction circuit and a line-like printhead. (5)

[0063]

[Effect of the Invention]

As described above, according to the present invention, a plurality of data sequences input with different data widths can be converted into output data sequences of prescribed data width without converting the input data sequences into serial data, and at the same time, the clock frequency used for the data sequence conversion can be held low. This serves to achieve a low-cost, high-speed operating data sequence conversion circuit. This data sequence conversion circuit is particularly suitable for use in an LED printer or the like.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

Figure 1 is a diagram schematically showing the construction of a printing section in an LED printer to which the data sequence conversion circuit of the present invention can be applied.

[Fig. 2]

Figure 2 is a diagram showing an LED array as viewed from the photosensitive drum side.

[Fig. 3]

Figure 3 is a diagram showing the configuration of a serial data input type LED array head.

[Fig. 4]

Figure 4 is a diagram showing the configuration of a parallel data input type LED array head.

[Fig. 5]

Figure 5 is a diagram showing the configuration of a jaggy correction circuit.

[Fig. 6]

Figure 6 is diagrams for explaining the operation of the jaggy correction circuit.

[Fig. 7]

Figure 7 is a block diagram for explaining the data sequence conversion circuit of the present invention in relation to other circuits.

[Fig. 8]

Figure 8 is a diagram showing the configuration of a prior art data sequence conversion circuit.

[Fig. 9]

Figure 9 is a diagram showing the configuration of one embodiment of a data sequence conversion circuit according to the present invention.

[Fig. 10]

Figure 10 is a timing chart for explaining a data sequence conversion operation from 5-bit width to 8-bit width.

[Fig. 11]

Figure 11 is a timing chart for explaining a data sequence conversion operation from 4-bit width to 8-bit width.

[Fig. 12]

Figure 12 is a timing chart for explaining a data sequence conversion operation from 3-bit width to 8-bit width.

[Fig. 13]

Figure 13 is a diagram showing the distributing output rule used in a switch matrix when performing the data sequence conversion from 5-bit width to 8-bit width.

[Fig. 14]

Figure 14 is a diagram showing the distributing output rule used in the switch matrix when performing the data

sequence conversion from 4-bit width to 8-bit width.

[Fig. 15]

Figure 15 is a diagram showing the distributing output rule used in the switch matrix when performing the data sequence conversion from 3-bit width to 8-bit width.

[Fig. 16]

Figure 16 is a diagram (1/5) showing an example of the circuit configuration of the switch matrix.

[Fig. 17]

Figure 17 is a diagram (2/5) showing an example of the circuit configuration of the switch matrix.

[Fig. 18]

Figure 18 is a diagram (3/5) showing an example of the circuit configuration of the switch matrix.

[Fig. 19]

Figure 19 is a diagram (4/5) showing an example of the circuit configuration of the switch matrix.

[Fig. 20]

Figure 20 is a diagram (5/5) showing an example of the circuit configuration of the switch matrix.

[Fig. 21]

Figure 21 is diagrams for explaining the simplified designations in the switch matrix circuit.

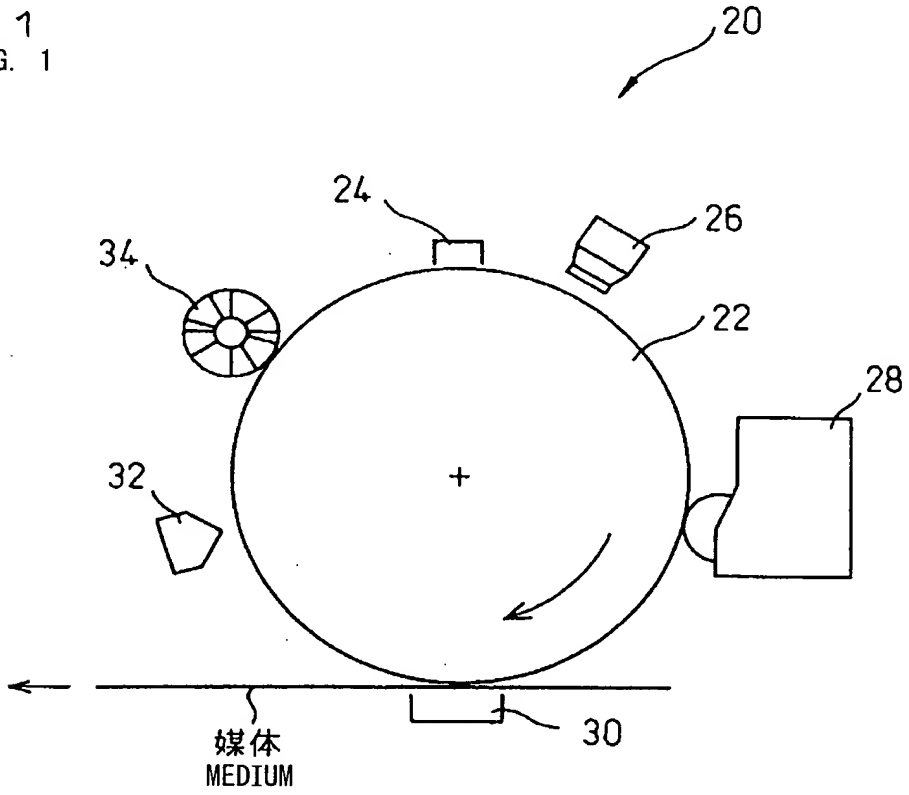
[Description of Reference Numerals]

20 ... printing section in an LED printer
22 ... photosensitive drum
24 ... charging unit
26 ... LED array head
28 ... developing unit
30 ... transfer unit
32 ... charge erasing unit
34 ... cleaner
40 ... LED array
42 ... LED driving circuit
44 ... serial shift register

46 ... parallel shift register
48 ... image memory
50 ... jaggy correction circuit
52 ... image memory reading unit
54 ... line buffer
56 ... evaluation window extracting unit
58 ... corrected image data generating unit
60 ... data sequence conversion circuit
62 ... parallel-to-serial conversion circuit
64 ... serial-to-parallel conversion circuit
72 ... input shift register
74 ... switch matrix
76 ... output shift register

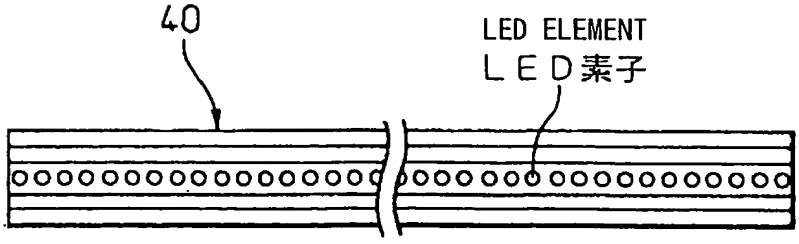
【書類名】　図面
[NAME OF DOCUMENT]　DRAWINGS
【図１】
[FIG. 1]

図１
FIG. 1



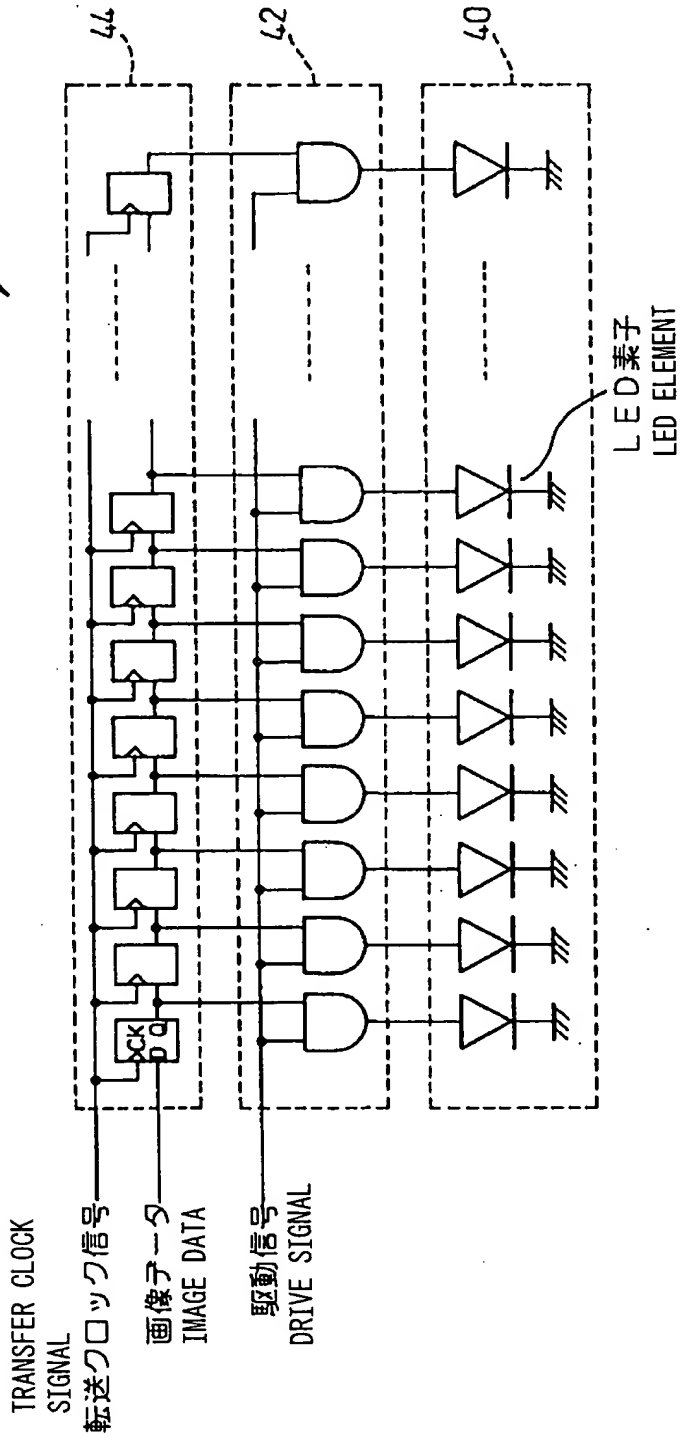
【図２】
[FIG. 2]

図２
FIG. 2



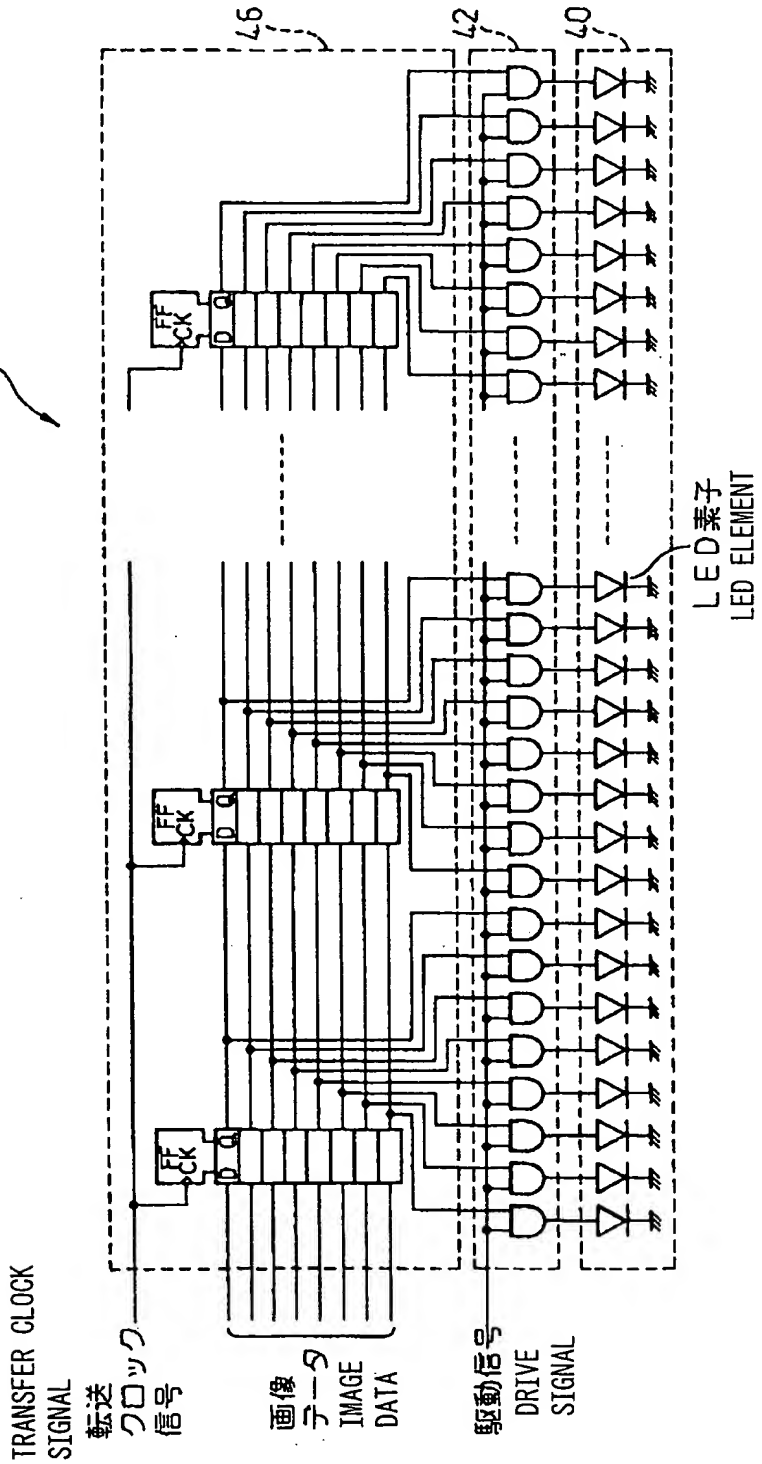
【図３】
[FIG. 3]

図３
FIG. 3



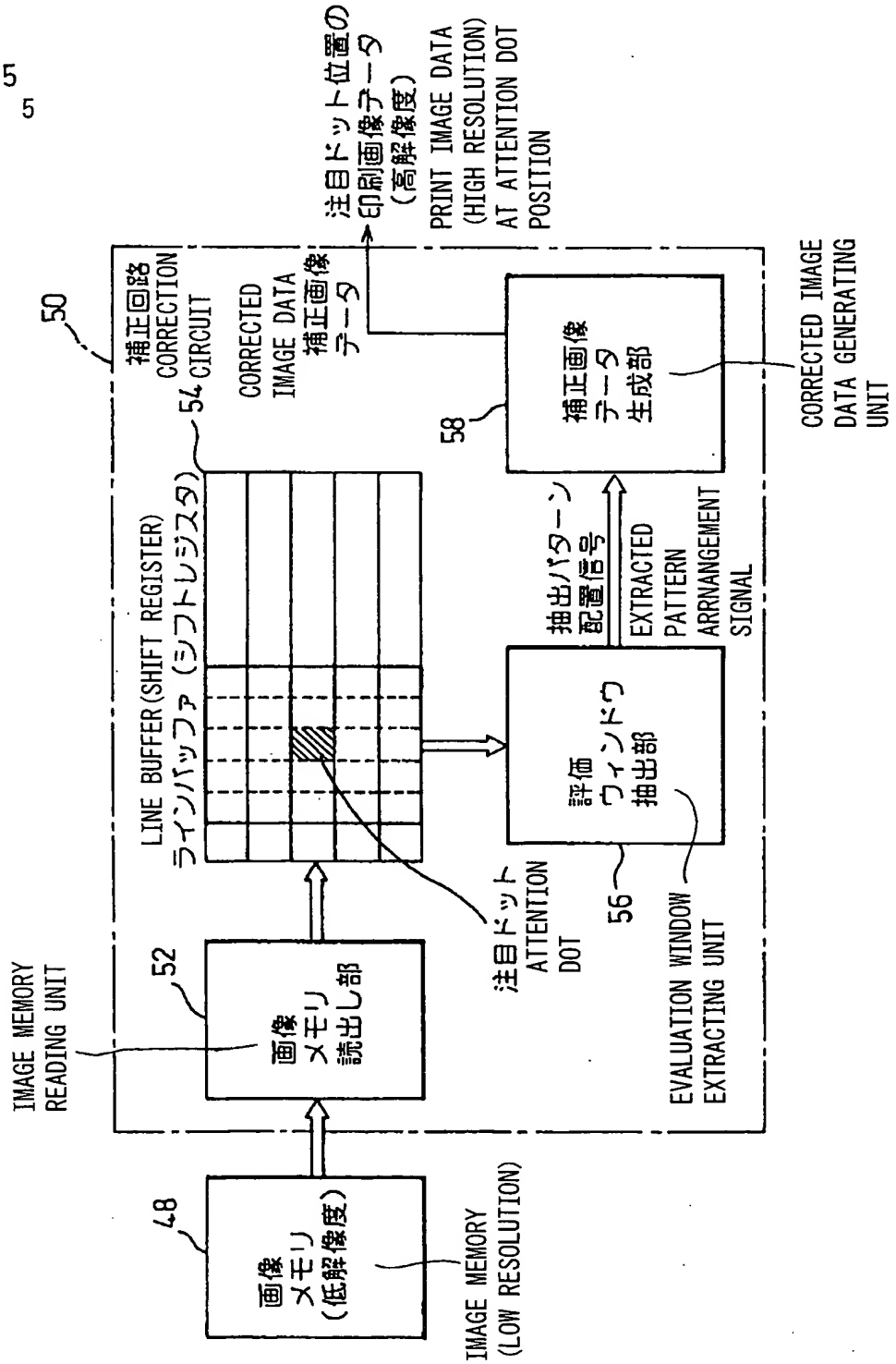
【図４】
[FIG. 4]

図４
FIG. 4



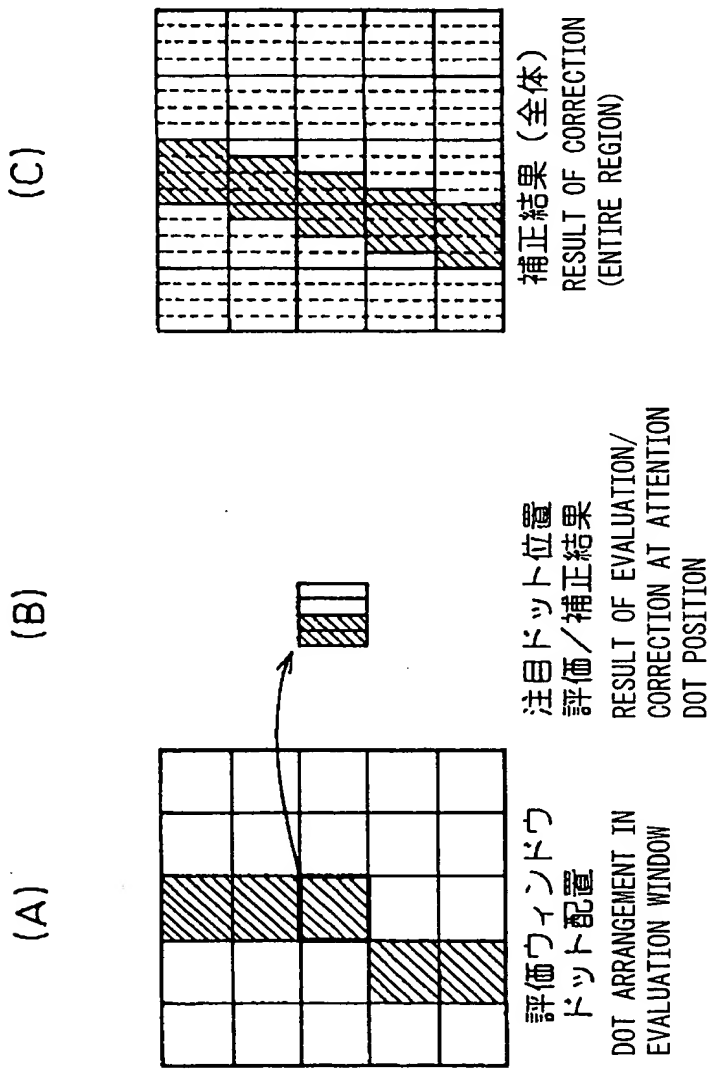
【図５】
[FIG. 5]

図 5
FIG. 5



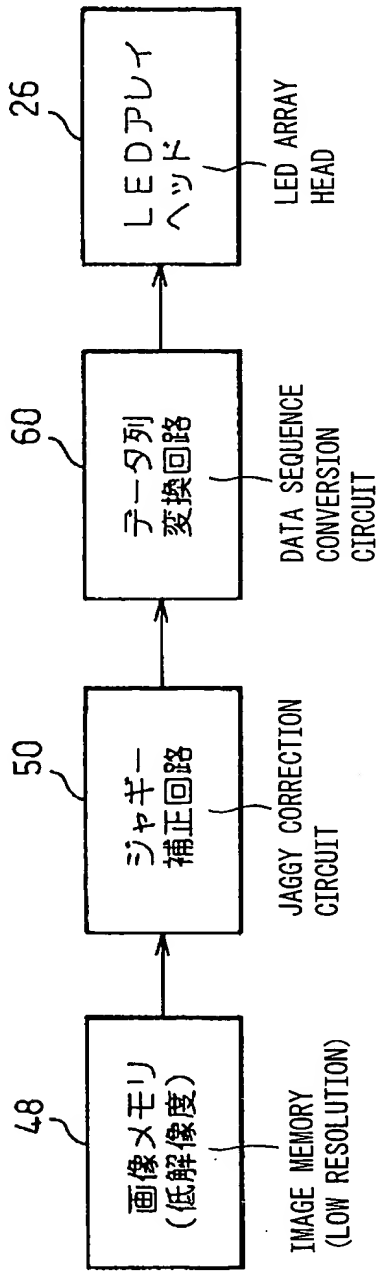
【図６】
[FIG. 6]

図 6
FIG. 6



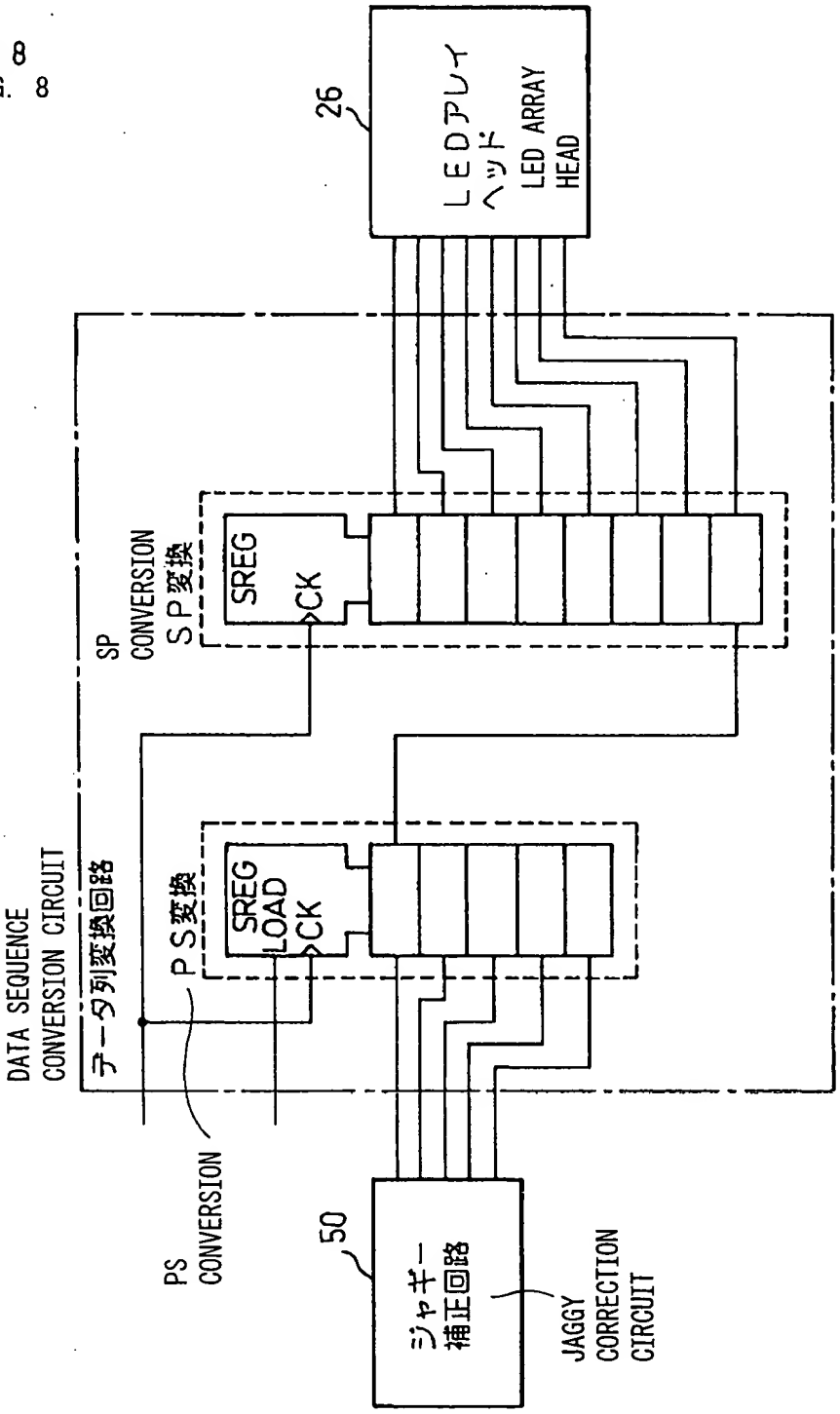
【図７】
[FIG. 7]

図 7
FIG. 7



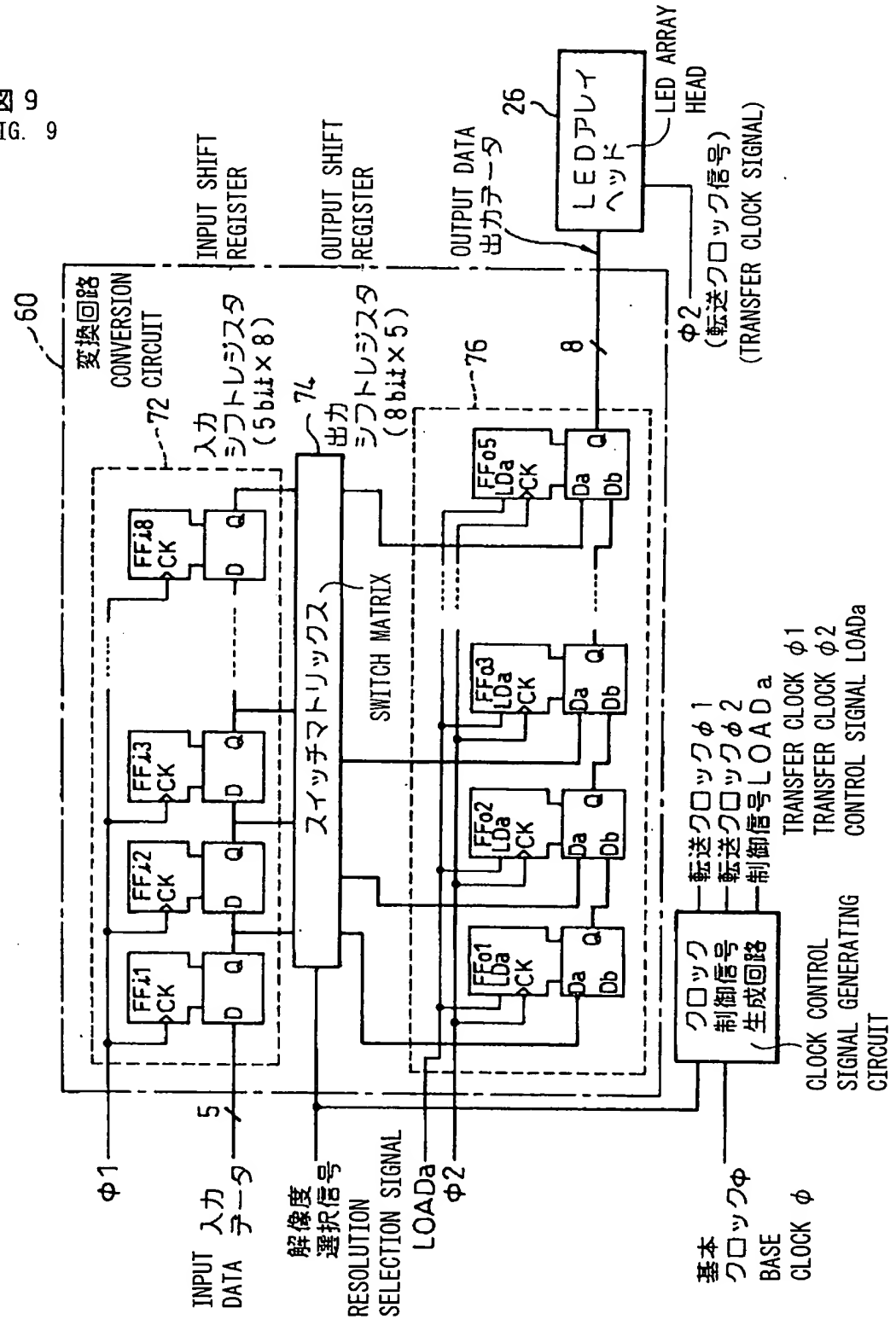
【図８】
[FIG. 8]

図８
FIG. 8



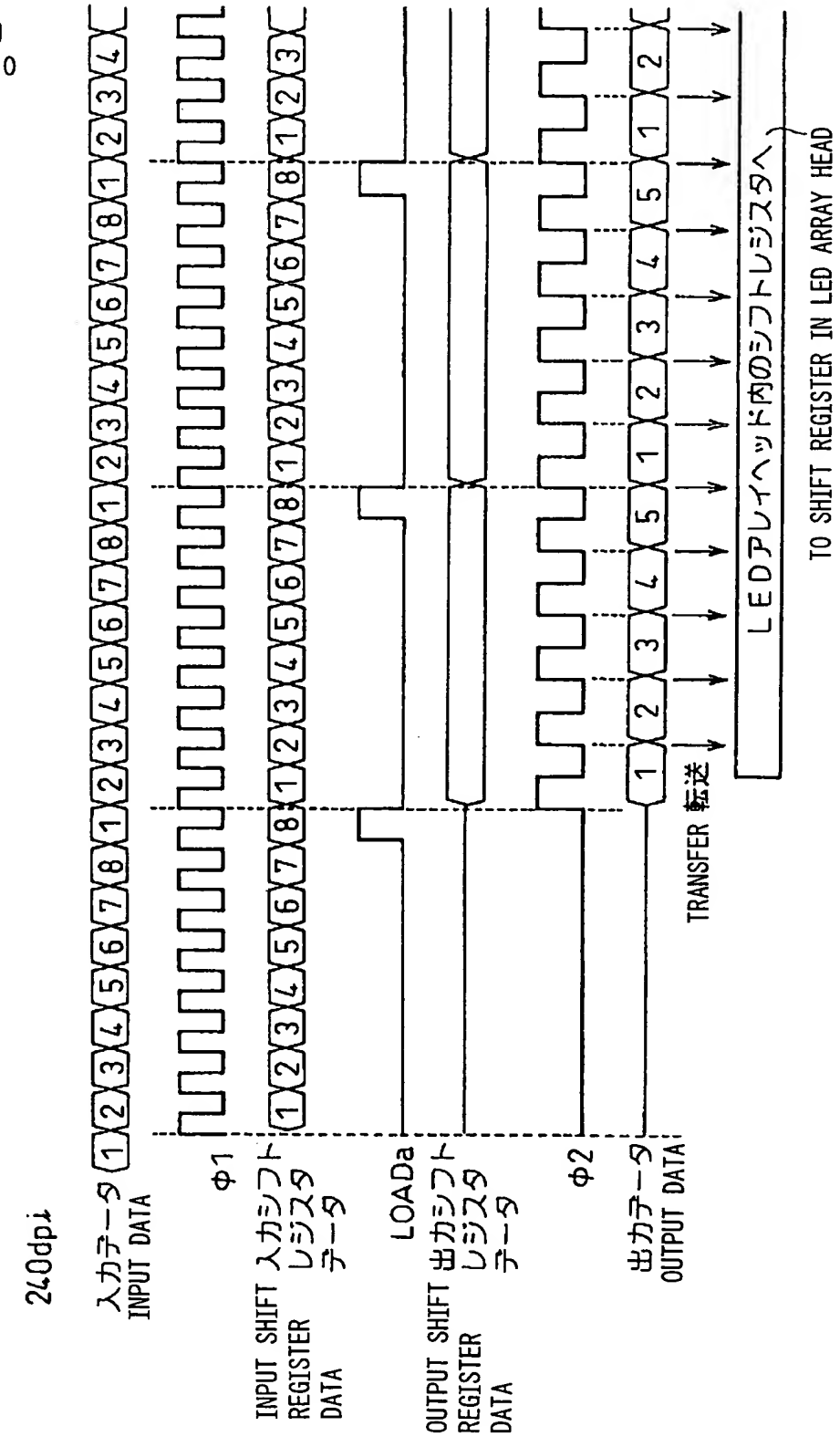
【図９】
[FIG. 9]

図９
FIG. 9



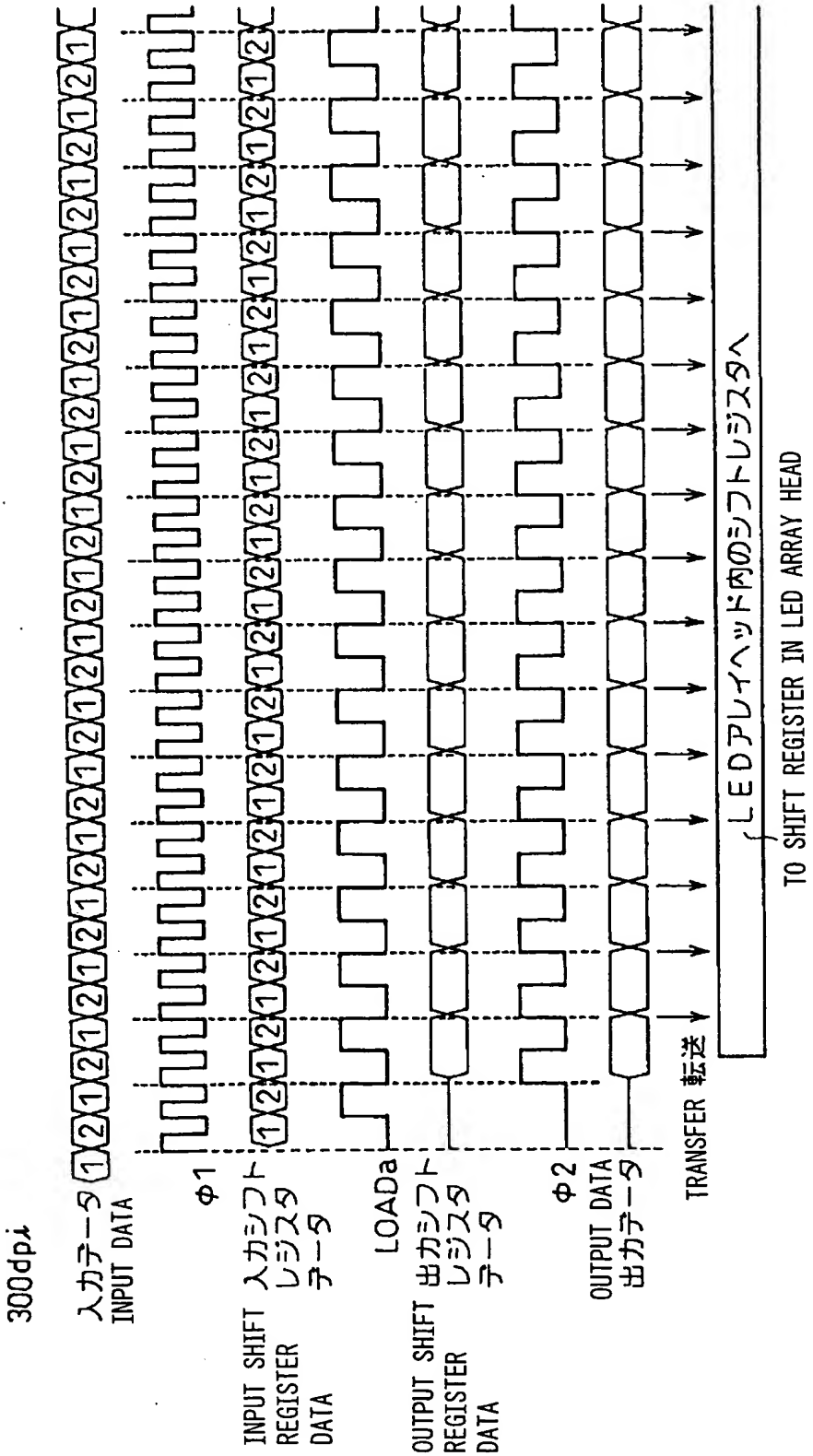
【図１０】
[FIG. 10]

図10
FIG. 10



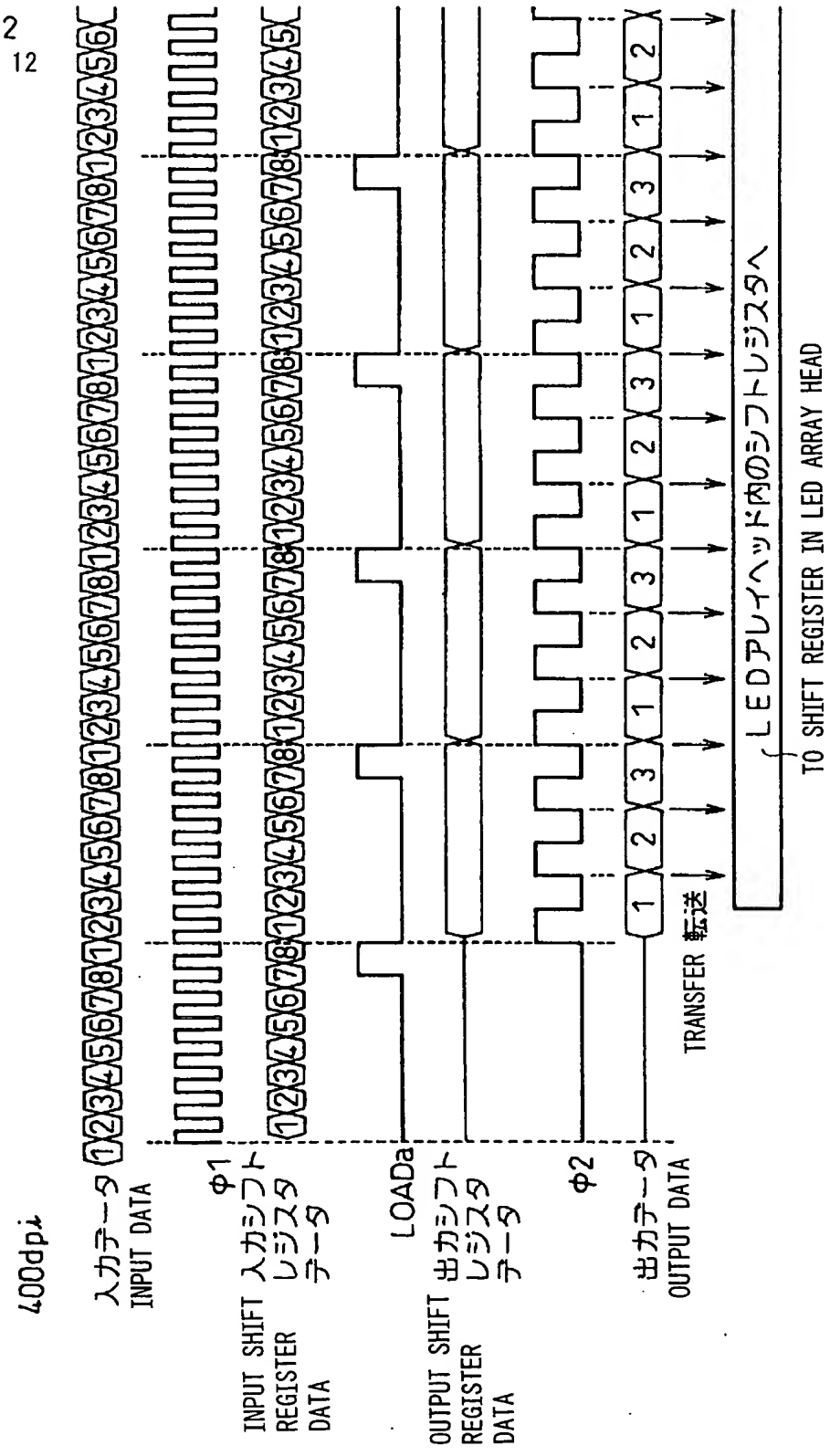
【図１１】
[FIG. 11]

図11
FIG. 11



【図１２】
[FIG. 12]

図12
FIG. 12



【図１３】
[FIG. 13]

図13
FIG. 13

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo1							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	FFi2 -Q2	FFi2 -Q1	FFi2 -Q0	FFi1 -Q4	FFi1 -Q3	FFi1 -Q2	FFi1 -Q1	FFi1 -Q0

OUTPUT SIGNAL

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo2							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	FFi4 -Q0	FFi3 -Q4	FFi3 -Q3	FFi3 -Q2	FFi3 -Q1	FFi3 -Q0	FFi2 -Q4	FFi2 -Q3

OUTPUT SIGNAL

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo3							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	FFi5 -Q3	FFi5 -Q2	FFi5 -Q1	FFi5 -Q0	FFi4 -Q4	FFi4 -Q3	FFi4 -Q2	FFi4 -Q1

OUTPUT SIGNAL

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo4							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	FFi7 -Q1	FFi7 -Q0	FFi6 -Q4	FFi6 -Q3	FFi6 -Q2	FFi6 -Q1	FFi6 -Q0	FFi5 -Q4

OUTPUT SIGNAL

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo5							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	FFi8 -Q4	FFi8 -Q3	FFi8 -Q2	FFi8 -Q1	FFi8 -Q0	FFi7 -Q4	FFi7 -Q3	FFi7 -Q2

OUTPUT SIGNAL

【図１４】
[FIG. 14]

図14
FIG. 14

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo1							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	×	×	×	×	×	×	×	×

OUTPUT SIGNAL

OUTPUT TERMINAL (DESTINATION)	出力端子（接続先）	FFo2							
		-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
OUTPUT SIGNAL	出力信号	×	×	×	×	×	×	×	×

OUTPUT TERMINAL (DESTINATION)	出力端子（接続先）	FFo3							
		-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
OUTPUT SIGNAL	出力信号	×	×	×	×	×	×	×	×

OUTPUT TERMINAL (DESTINATION)	出力端子（接続先）	FFo4							
		-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
OUTPUT SIGNAL	出力信号	×	×	×	×	×	×	×	×

OUTPUT TERMINAL (DESTINATION)	出力端子（接続先）	FFo5							
		-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
OUTPUT SIGNAL	出力信号	FFi2 -Q3	FFi2 -Q2	FFi2 -Q1	FFi2 -Q0	FFi1 -Q3	FFi1 -Q2	FFi1 -Q1	FFi1 -Q0

【図１５】
[FIG. 15]

図15
FIG. 15

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo1							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	×	×	×	×	×	×	×	×

OUTPUT SIGNAL

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo2							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	×	×	×	×	×	×	×	×

OUTPUT SIGNAL

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo3							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	FFi3 -Q1	FFi3 -Q0	FFi2 -Q2	FFi2 -Q1	FFi2 -Q0	FFi1 -Q2	FFi1 -Q1	FFi1 -Q0

OUTPUT SIGNAL

OUTPUT TERMINAL (DESTINATION)

出力端子（接続先）	FFo4							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	FFi6 -Q0	FFi5 -Q2	FFi5 -Q1	FFi5 -Q0	FFi4 -Q2	FFi4 -Q1	FFi4 -Q0	FFi3 -Q2

OUTPUT SIGNAL

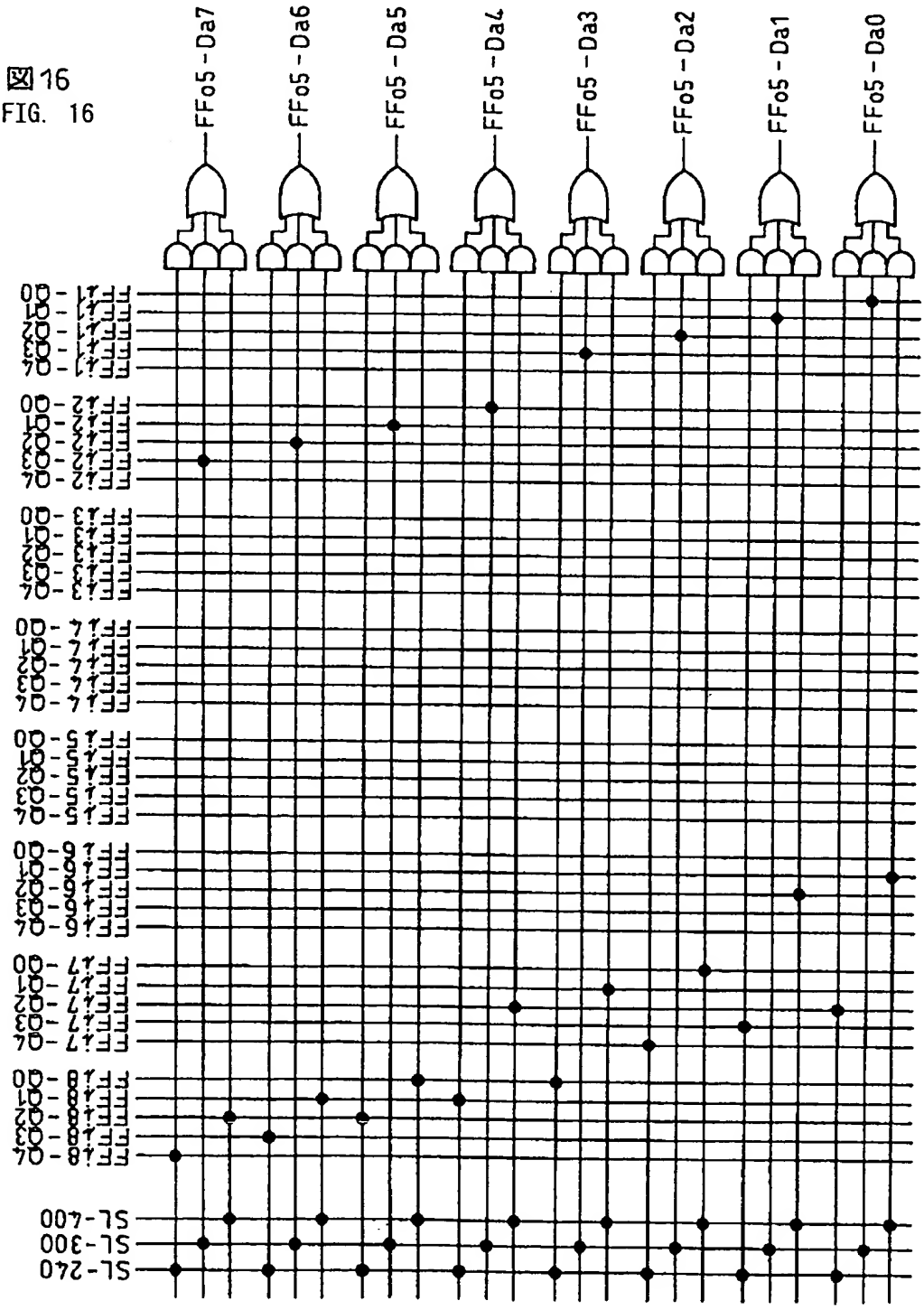
出力端子（接続先）	FFo5							
	-Da7	-Da6	-Da5	-Da4	-Da3	-Da2	-Da1	-Da0
出力信号	FFi8 -Q2	FFi8 -Q1	FFi8 -Q0	FFi7 -Q2	FFi7 -Q1	FFi7 -Q0	FFi6 -Q2	FFi6 -Q1

OUTPUT TERMINAL (DESTINATION)

OUTPUT SIGNAL

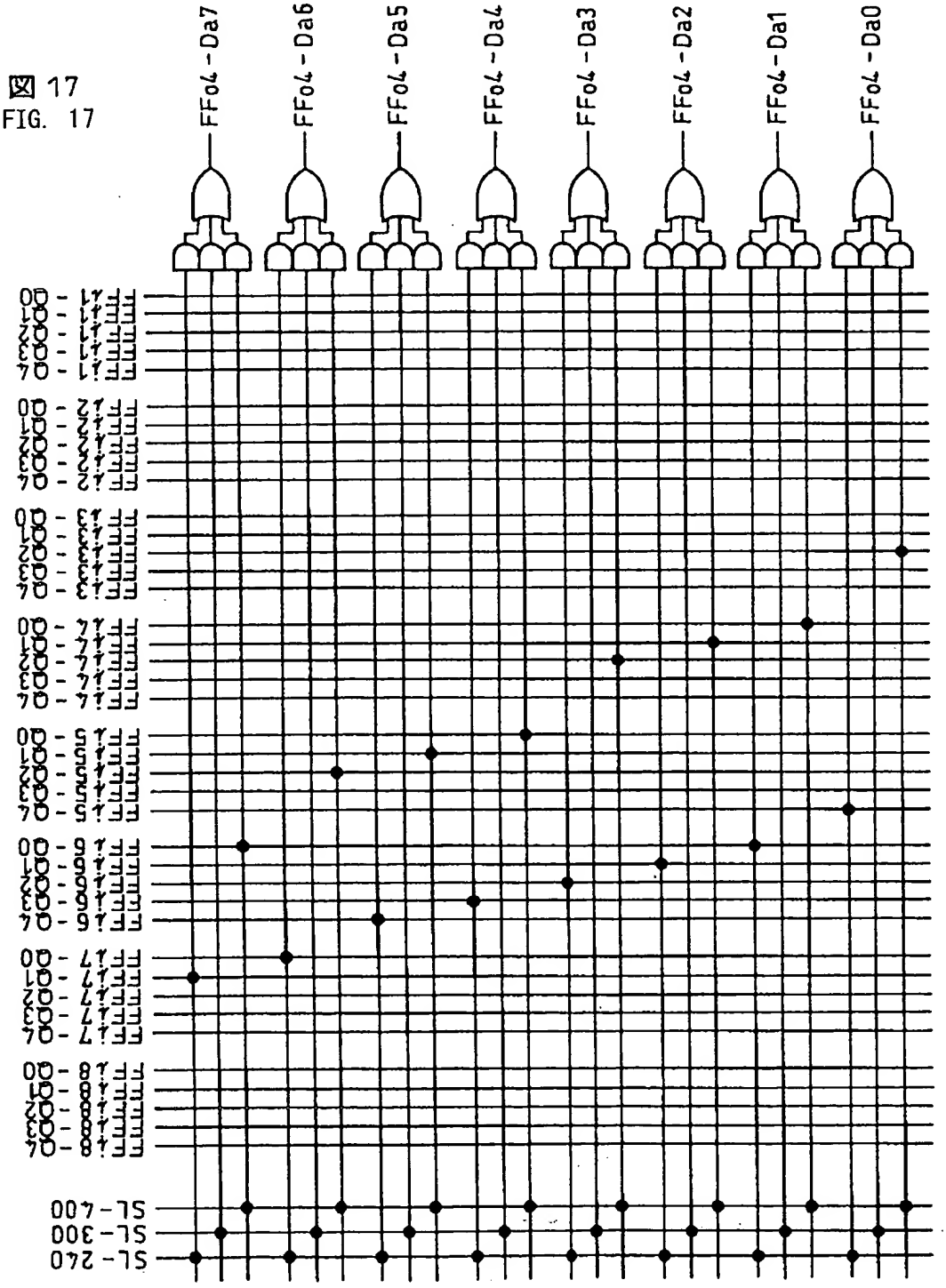
【図１６】
[FIG. 16]

図16
FIG. 16



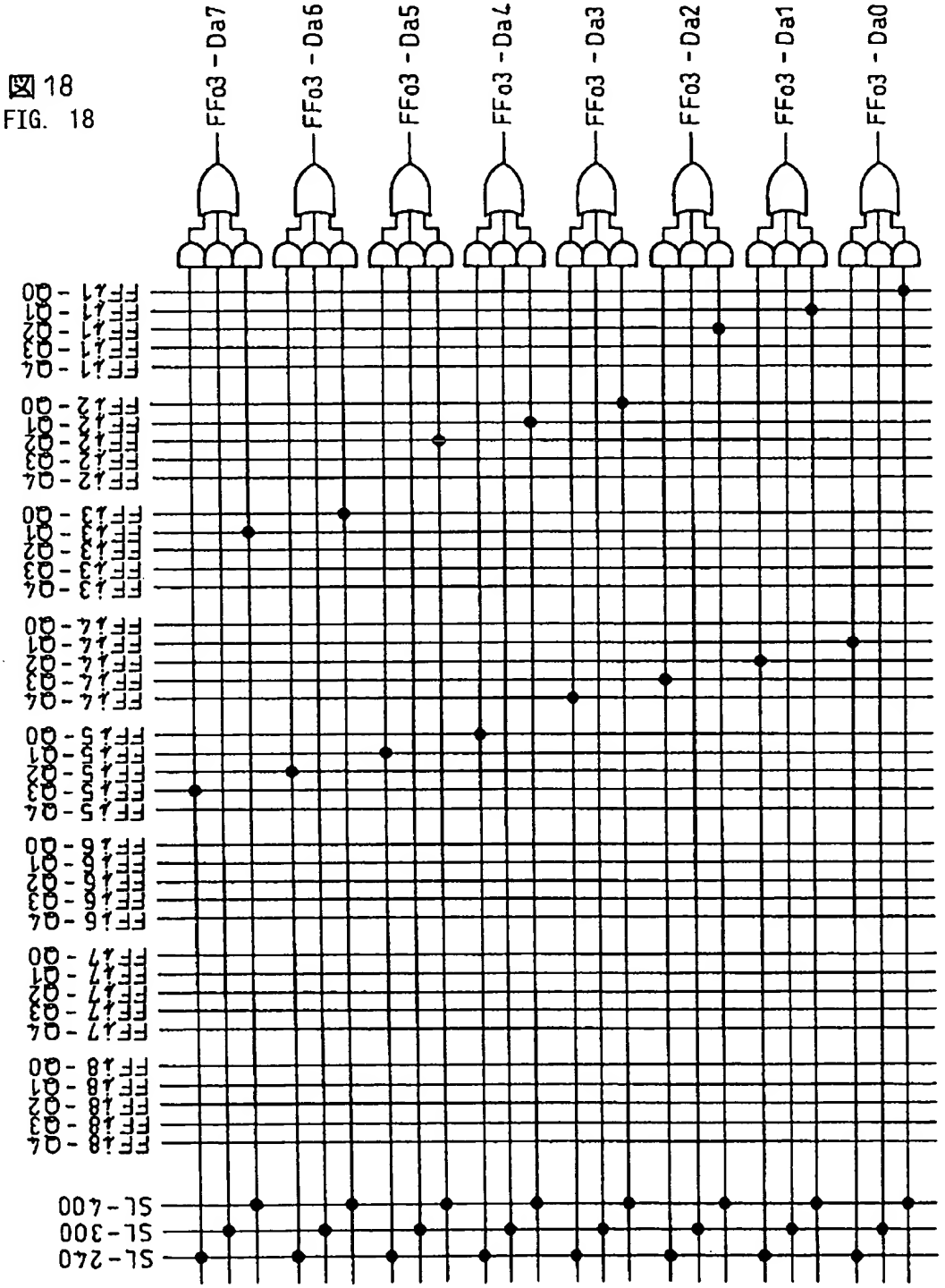
【図１７】
[FIG. 17]

図 17
FIG. 17



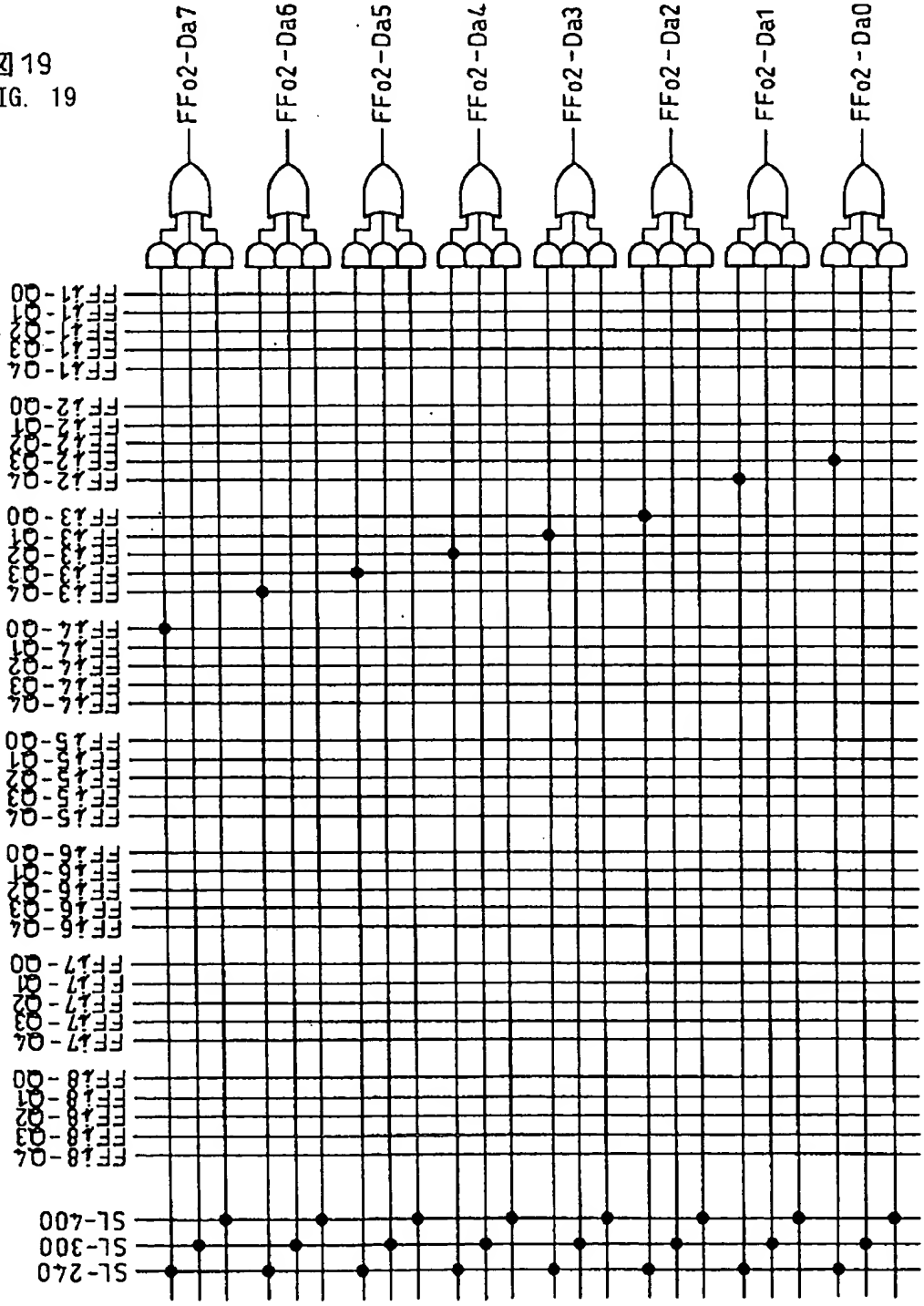
【図１８】
[FIG. 18]

図18
FIG. 18



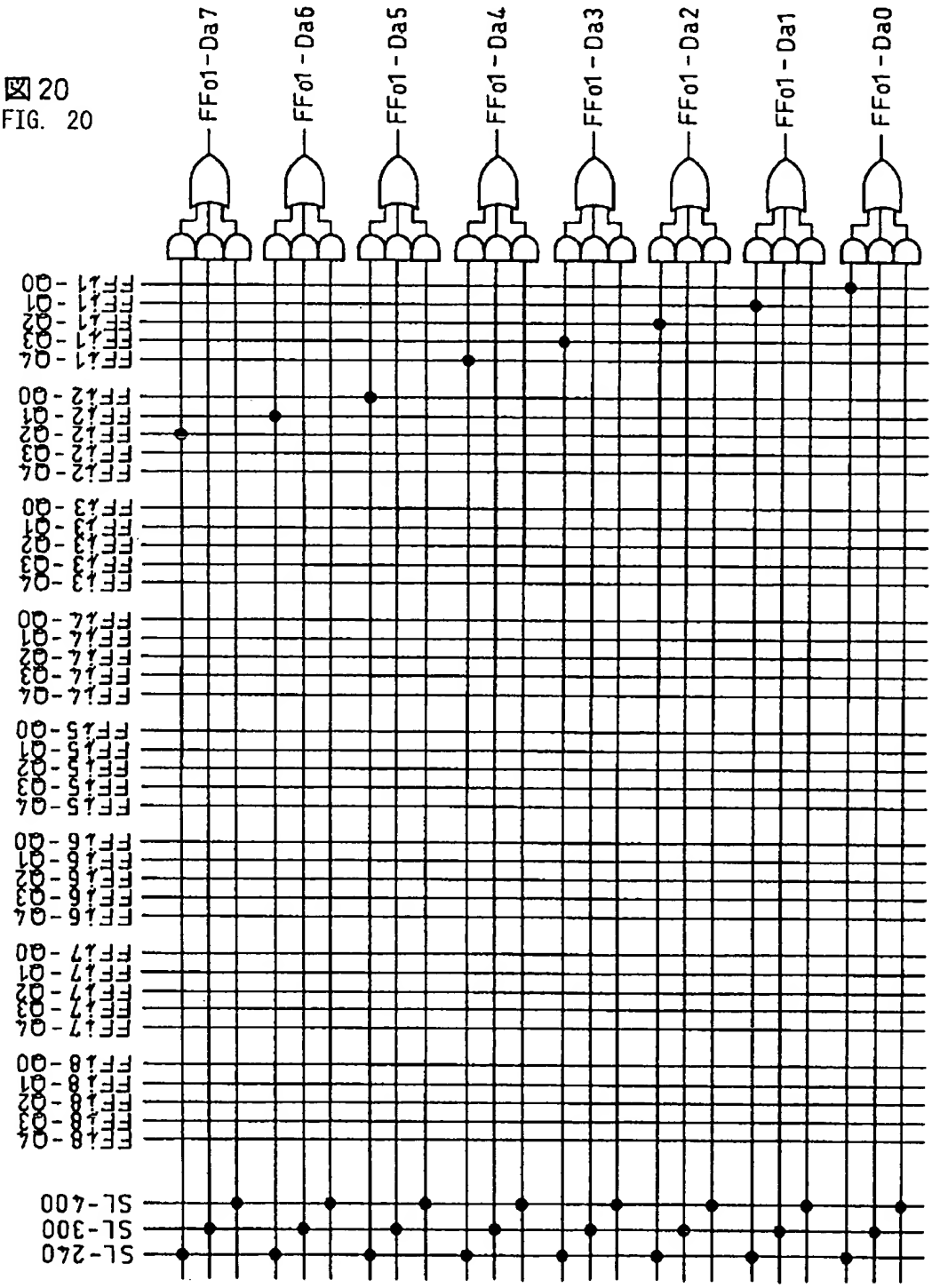
【図１９】
[FIG. 19]

図19
FIG. 19



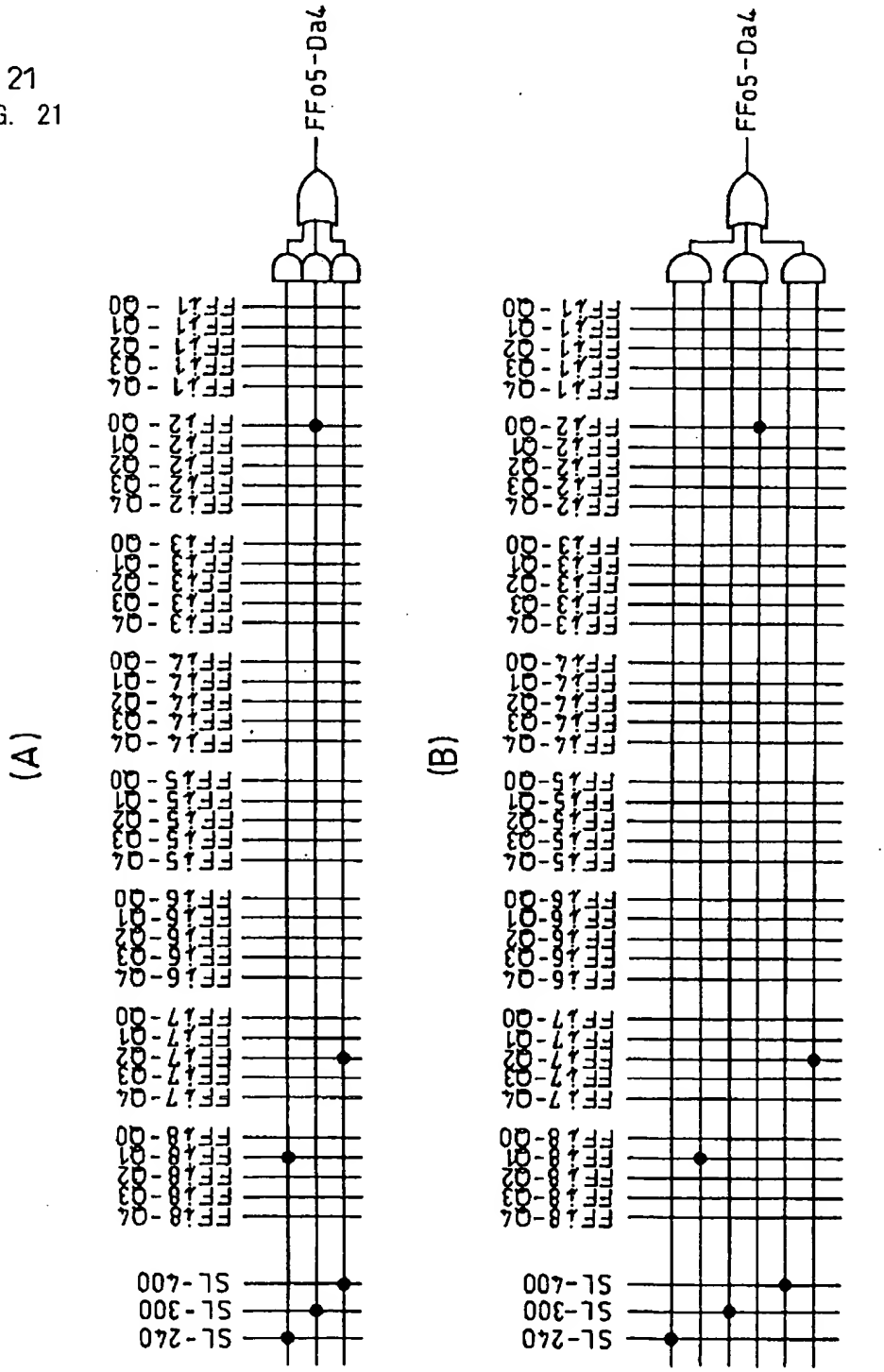
【図２０】
[FIG. 20]

図20
FIG. 20



【図２１】
[FIG. 21]

図21
FIG. 21



[NAME OF DOCUMENT] ABSTRACT

[ABSTRACT]

[PROBLEM] To convert a plurality of input data sequences having different data widths into output data sequences having a prescribed data width without converting the input data sequences into serial data.

[SOLUTION MEANS] The data sequence conversion circuit, which takes as an input any one of a plurality of input data sequences having different data widths and converts the input data sequence into an output data sequence having a prescribed data width for output, includes: a first parallel shift register 72 for holding the input data sequence; a switch matrix 74 for taking the data held in the first parallel shift register as input data, and for outputting the input data in distributing fashion in accordance with a rule selected by a control signal from a plurality of predetermined rules; and a second parallel shift register 76 for taking the data output from the switch matrix as input data, and for outputting the input data as a data sequence having the prescribed data width.

[SELECTED DRAWING] Figure 9